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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,081	08/22/2003	Ravindraraj Ramaraju	SC12814TC	9610

23125 7590 10/31/2006

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EXAMINER	
WELLS, KENNETH B	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,081	RAMARAJU ET AL.	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6 and 8-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4, 6 and 8-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. The appeal brief filed on 9/21/06 has been received and entered in the case. In view of the arguments therein, the previous rejections are withdrawn and replaced with new rejections, based on the same prior art.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 4, 6 and 8-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Weiberneit et al.

See paragraph five of the previous office action mailed on 12/1/05 for the details of this reference. As to the limitation that the input signals are both in the same logic state when the clock is high (the recited second clock state), this will be inherent during the operation of the Weiberneit et al Fig. 3 circuitry. Applicant's assertion that the logic state of the signal received by inverter E will always be complementary to the logic state of the signal received by inverter S2 is incorrect, i.e., because of the inherent delay associated with passing a signal through an inverter (such as inverter S1 in Weiberneit et al's Fig. 3), there will always be an offset between the high-to-low pulse of the input to inverter E and the low-to-high pulse of the input to inverter S2. Stated

differently, when the I3 signal (input to inverter E) goes from "1" to "0", the /I3 signal (input to inverter S2) will go from "0" to "1" at a slightly delayed point in time. In view of this well-known relationship between the signal at the input of an inverter and the signal at the output of the inverter, there will necessarily be a slight interval where the input to the inverter has fallen to the low logic state prior to the output of the inverter transitioning to the high logic state. During this slight time interval, both the input and the output of the inverter will both be logic low, i.e., at the same logic state. Note also that such will also occur when the input to the inverter is going from "0" to "1" and the output is delayed in going from "1" to "0" (there will again be a slight time interval when both the input and output of the inverter are high logic level). The relationship of the high/low logic levels of the clock signal with respect to the data and data complement signals will be the same as in applicant's Fig. 4, i.e., when the clock is high, the input and output of inverter S1 will at times be complementary (one high, the other low), and at other times be at the same logic state (as noted above, due to the inherent delay caused by inverter S1).

4. Claims 1, 4, 6 and 8-15 are rejected under 35 U.S.C. 102(b)

as being anticipated by Lin.

Note Fig. 12, where the first clocked inverters (corresponding to applicant's circuits 200 and 210) are the inverters within section 170, and the second clocked inverters (corresponding to applicant's circuits 220 and 230) are the inverters within section 172. The analysis above with respect to the clocking and data timing of the Weiberneit et al Fig. 3 circuit likewise applied to the clocking and data timing of the Lin Fig. 12 circuitry.

5. Claims 1, 4, 6 and 8-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weiberniet et al or Lin.

To the extent that the clocking and data timing recited in the claims is not inherent in Weiberneit et al and Lin, it nevertheless would have been obvious to any person having ordinary skill in the art who of course can set the data and clocking timing in any manner desired, simply using well-known delay and/or synchronization techniques. It is noted that applicant admits this fact and also discusses well-known reasons (motivation) for forcing the data and /data signals to be at the same logic state in the background section of the instant specification. See, for example, paragraph [0015] and the discussion of well-known domino logic data synchronization where

applicant discusses in detail the desirability of forcing the data and data complement signals to be at the same logic state during the precharging of latches used in domino logic circuits.

6. In view of the above-noted new grounds of rejection, this action is non-final.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system,

see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

October 28, 2006